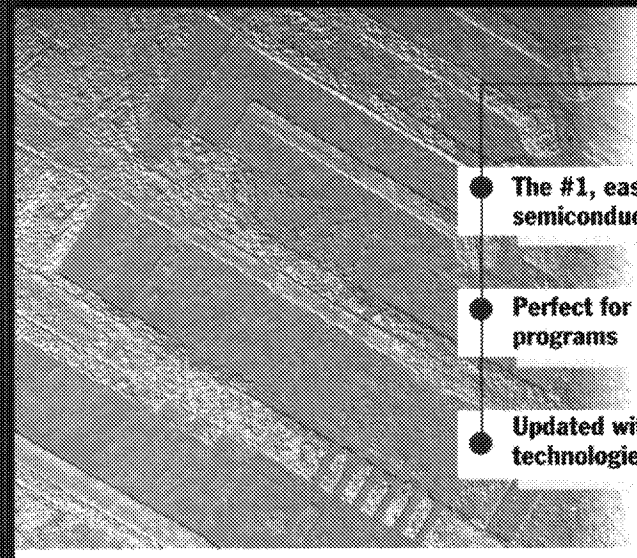
EXHIBIT 10

The #1 book in the industry — now revised & updated!



- The #1, easy-to-read, math-free introduction to semiconductor processing
- Perfect for training, teaching, & vo-tech programs
- Updated with new cleaning techniques, packing technologies, & fabrication methods

FOURTH EDITION

Microchip Fabrication

A Practical Guide to SEMICONDUCTOR PROCESSING

PETER VAN ZANT

Microchip Fabrication

A Practical Guide to Semiconductor Processing

Peter Van Zant

Fourth Edition

McGraw-Hill

New York San Francisco Washington, D.C. Auckland Bogotá
Caracas Lisbon London Madrid Mexico City Milan
Montreal New Delhi San Juan Singapore
Sydney Tokyo Toronto

Library of Congress Cataloging-in-Publication Data

Van Zant, Peter.
Microchip fabrication : a practical guide to semiconductor processing / Peter Van Zant.—4th ed.
p. cm.
Includes bibliographical references and index.
ISBN 0-07-135636-3
1. Semiconductors—Design and construction. I. Title.
TK7871.85.V36 2000
621.3815'2—dc21

00-02317

McGraw-Hill
A Division of The McGraw-Hill Companies

1 2 3 4 5 6 7 8 9 0 DOC/DOC 0 9 8 7 6 5 4 3 2 1 0

ISBN 0-07-135636-3

The sponsoring editor for this book was Stephen Chapman and the production supervisor was Sherri Souffrance. It was set in Century Schoolbook by Pro-Image Corporation.

Printed and bound by R. R. Donnelley & Sons Company.

This book is printed on recycled, acid-free paper containing a minimum of 50% recycled, de-inked fiber.

Many thanks to Mary DeWitt, my ever patient and supportive wife, and my sons, Patrick, Jeffrey, and Stephen. They have all brought great joy to my life and all have managed to live through the demands of my microelectronics career. Thank you.

Contents

Chapter

12

Deposition

Overview

While the doped regions and N/P junctions comprise the elecrically active components in a circuit, it takes various other layers of semiconductors, dielectrics, and conductors to complete the device/circuit. Many are depositied on the wafer by chemical vapor techniques (CVD) or by physical vapor deposition (PCD). This chapter describes the most commonly used CVD techniques and materials deposited on the wafer surface.

Objectives

Upon completion of this chapter, you should be able to:

1. Name the parts of a CVD reactor.
2. Describe the principle of chemical vapor deposition.
3. List the conductor, semiconductor, and insulator materials deposited by CVD techniques.
4. Know the difference between atmospheric CVD, LPCVD, hot-wall, and cold-wall systems.
5. Explain the difference between epitaxial and polysilicon layers.

Introduction

Advances in photomasking technology have allowed the fabrication of VLSI/ULSI circuits. But as the circuits have shrunk they also have grown in the vertical direction, through increased numbers of depos-

ited layers. In the 1960s bipolar devices had two layers deposited by chemical vapor deposition (CVD), an epitaxial layer and a top side passivation layer of silicon dioxide (Fig. 12.1) while early MOS devices had just a passivation layer (Fig. 12.2). By the 1990s, advanced devices featured four levels of metal interconnects requiring numerous deposited layers. The added layers take a variety of roles in the device/circuit structures. Primary ones are deposited doped silicon layers called epitaxial layers (see section in this chapter), intermetal dielectrics (IMD), intermetal conducting plugs, metal conducting layers, and final passivation layers. Figure 12.3 lists common layers deposited. There are two primary techniques for layer deposition: chemical vapor deposition and physical vapor deposition (PVD). The PVD techniques of evaporation and sputtering are explained in Chapter 13. The uses of the particular films, while indicated in this chapter, are detailed in Chapters 16 and 17. Chemical vapor deposition (CVD), the subject of this chapter, is practiced in a number of atmospheric and low pressure techniques.

Film parameters

Device layers must meet general and specific parameters. The specific parameters is noted in the sections on individual layer materials. General criteria that all films must meet for semiconductor use include:

- Thickness/uniformity
- Surface flatness/roughness
- Composition/grain size

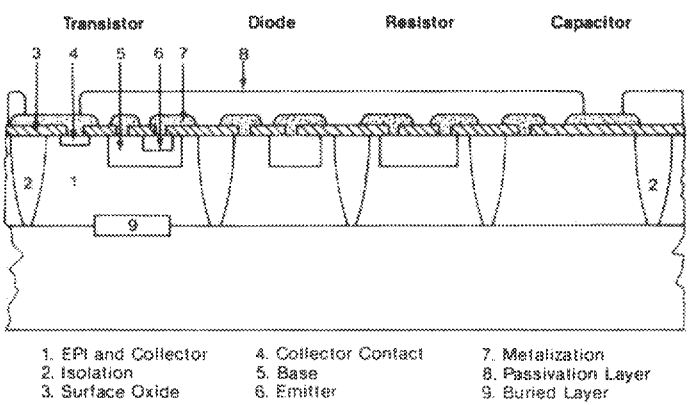


Figure 12.1 Cross section of bipolar circuit showing epitaxial layer and isolation.

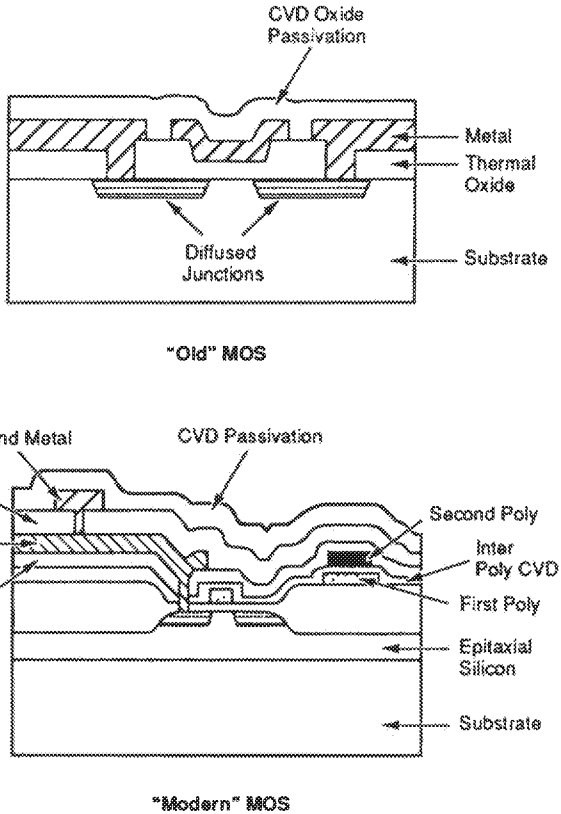


Figure 12.2 Evolution of MOS layers.

Atmospheric Pressure (AP)	Low Pressure (LP) and Ultra High Vacuum (UHV)
Cold wall • Horizontal • Vertical • Barrel • Vapor phase epitaxy Metalorganic CVD	Hot wall Plasma enhanced Vertical isothermal Molecular beam epitaxy (MBE)

Figure 12.3 Overview of deposition systems.

- Stress free
- Purity
- Integrity

Uniform thickness is required of films to meet both electrical and mechanical specifications. Deposited films must be continuous and free of pinholes to prevent the passage of contamination and to prevent shorting of sandwiched layers. This is of great importance for thin films. Epitaxial films have shrunk from 5-μm levels to submicron thicknesses. Recall that the thickness of a layer is one of the factors contributing to its resistance. Also, thinner layers tend to have more pinholes and less mechanical strength. Of particular concern is the maintenance of thickness over steps (Fig. 12.4). Excessive thinning at a step can cause electrical shorts and/or unwanted induced charges in the device. The problem becomes very acute in deep and narrow holes and trenches, called high aspect ratio patterns. The ratio is calculated by dividing the depth by the width (Fig. 12.4). One problem is a thinning of the deposited film at the lip of the trench. Another is thinning in the bottom of the trench. Filling high aspect trenches is a major issue in the execution of multimetal structures.

Surface flatness is as important as the thickness. In Chapter 10, the effect of steps and surface roughness on image formation was detailed. Deposited films must be flat and as smooth as the material and deposition method will allow to minimize steps, cracking, and subsurface reflections.

Deposited films must be of the desired uniform composition. Some of the reactions are complex and it is possible that films will be deposited with different than the intended composition. Stoichiometry is the methodology by which the quantities of reactants and products in chemical reactions are determined. In addition to chemical composition, grain size is important. During deposition, the film materials tend to collect or grow into grains. Varying grain size within films of the same composition and thickness will yield different electrical and mechanical properties. This is because electrical current flow is af-

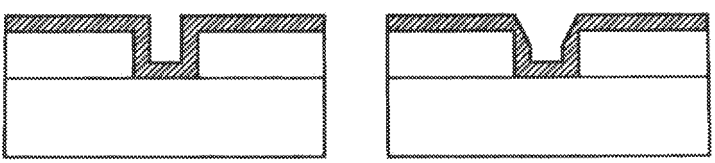


Figure 12.4 Thinning of deposited layer (*b*) at step.

fected as it passes through the grain interfaces. Mechanical properties also change with the size of grain interface area.

Stress-free films are another requirement. A film deposited with excess stress will relieve itself by forming cracks. Cracked films cause surface roughness and can allow contamination to pass through to the wafer. In the extreme they cause electrical shorts.

Purity, that is, no unwanted chemical elements or molecules in the film, is required for the film to carry out its intended function. For example, oxygen contamination of an epitaxial film will change its electrical properties. Purity also includes the exclusion of mobile ionic contaminants and particulates.

An electrical parameter of importance to deposited films is capacitance (see Chapter 2). Semiconductor metal conduction systems need high conductivity and, therefore, low resistance and low capacitance materials. These are referred to as low-k dielectrics. Dielectric layers used as insulators between conducting layers need high capacitances or high-k dielectrics.

Chemical Vapor Deposition Basics

Not surprisingly, the growth in the number and kinds of deposited films has resulted in a number of deposition techniques. Where the process engineer of the 1960s had a choice of only atmospheric chemical vapor deposition (CVD), today's engineer has many more options (Fig. 12.3). These techniques are described in the following sections.

Thus far the terms *deposition* and *CVD* have been used without explanation. In semiconductor processing, deposition refers to any process in which a material is physically deposited on the wafer surface. Grown films are those, such as silicon dioxide, that formed from the material in the wafer surface. The majority of films are deposited by a CVD technique. In concept, the process is simple (Fig. 12.5). Chemicals (C) containing the atoms or molecules required in the final film are mixed and reacted in a deposition chamber to form a vapor (V). The atoms or molecules deposit (D) on the wafer surface and build up to form a film. Figure 12.5 illustrates the reaction of silicon tetrachlo-

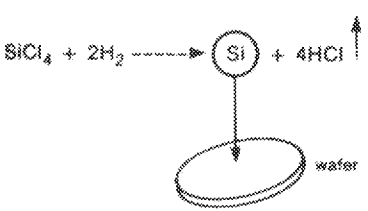


Figure 12.5 Chemical vapor deposition of silicon from silicon tetrachloride.

ride ($SiCl_4$) with hydrogen to form a deposited layer of silicon on the wafer. Generally, CVD reactions require the addition of energy to the system, such as heating the chamber or the wafer.

The chemical reactions that take place fall into the four categories of pyrolysis, reduction, oxidation, and nitridation (Fig. 12.6). Pyrolysis is the process of chemical reaction driven by heat alone. Reduction causes a chemical reaction by reacting a molecule with hydrogen. Oxidation is the chemical reaction of an atom or molecule with oxygen. Nitridation is the chemical process of forming silicon nitride.

Deposited film growth proceeds in several distinct stages (Fig. 12.7) The first stage, *nucleation*, is very important and critically dependent on substrate quality. Nucleation occurs as the first few atoms or molecules deposit on the surface. These first atoms or molecules form islands that grow into larger islands. In the third stage the islands spread, finally coalescing into a continuous film. This is the transition stage of the film growth with a typical thickness of several hundred angstroms. The transition region film has chemical and physical properties much different than the final, thicker "bulk" film.[1]

After the transition film is formed, the growth of the bulk begins. Processes are design to produce on of three structures: amorphous, polycrystalline, and single crystal (Fig. 12.8). These terms have been defined before. A poorly defined or controlled process can result in a film with the wrong structure. For example, attempting to grow a single-crystal epitaxial film on a wafer with islands of unremoved oxide will result in regions of polysilicon in the bulk film.

Pyrolysis	$SiH_4 \rightarrow Si + 2H_2$
Reduction	$SiCl_4 + 2H_2 \rightarrow Si + 4HCL$
Oxidation	$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$
Nitridation	$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + pH + 6H_2$

Figure 12.6 Examples of CVD reactions.

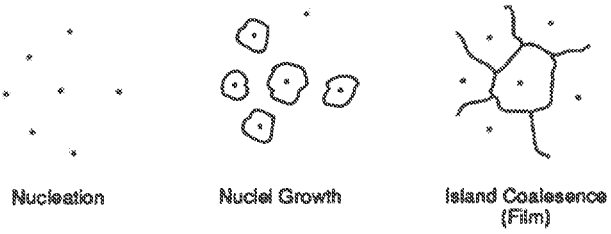


Figure 12.7 CVD film growth steps.

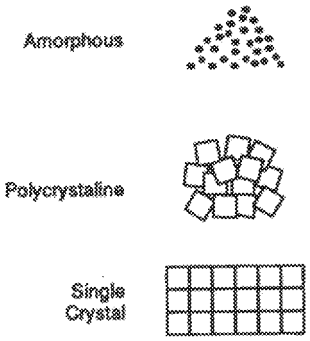


Figure 12.8 Types of film structure.

Basic CVD system design

CVD systems come in a wide variety of designs and options. Understanding the many variations is helped by an examination of the basic subsystems common to most CVD systems (Fig. 12.9). In most respects, a CVD system has the same basic parts as a tube furnace (described in Chapter 7): source cabinet, reaction chamber, energy source, wafer holder (boat), and loading and unloading mechanisms. In some cases, the CVD system *is* a tube furnace identical to those used for oxidation and diffusion. The source chemicals are housed in a source section. Vapors are generated from pressurized gas cylinders or liquid source bubblers. Gas flow control is maintained by pressure regulators, mass flow meters, and timers.[2]

The actual deposition takes place on the wafers in a reaction chamber. Most reactions require an energy source that heats the chamber or the wafers directly. Energy sources are either heat (conduction-

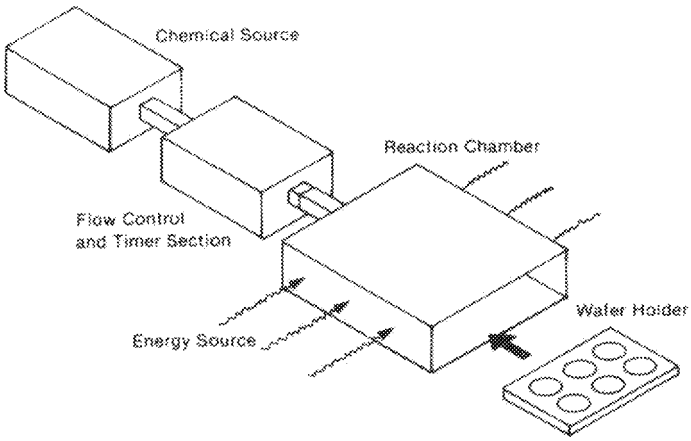


Figure 12.9 Basic CVD subsystems.

convection), induction RF, radiant, plasma, or ultraviolet. Energy sources are explained in the sections on particular systems. Temperatures range from room temperature to 1250°C depending on the reaction, film thickness required, and the growth parameters.

The fourth basic part of the system is the wafer holder. Different chamber configurations and heat sources dictate the style and material of the holders. Most production-level systems for VLSI work are automated from wafer load to unload. A full production system will have an associated cleaning section or station and a loading area.

CVD Process Steps

A CVD process follows the same steps as an oxidation or diffusion process. For review, the steps are preclean (and etch, if required), deposition, and evaluation. Cleaning processes are those already described to remove particulates and mobile ionic contaminants. Chemical vapor deposition, like an oxidation, take place in cycles. First the wafers are loaded into the chamber, usually with an inert atmosphere. Next the wafers are brought to temperature. Chemical vapors are introduced for as long as required to deposit the film. Finally the chemical source vapors are flushed out and the wafers removed. Evaluation of the films are for thickness, step coverage, purity, cleanliness, and composition. Evaluation techniques are explained in Chapter 14.

CVD System Types

CVD systems (Fig. 12.3) are divided into two primary types: atmospheric pressure (AP) and low pressure (LP). There are a number of atmospheric pressure CVD systems (APCVD). Most advanced device films are deposited in systems where the pressure has been lowered. These are called low pressure CVD or LPCVD.

Another differentiation is cold wall or hot wall. Cold-wall systems directly heat the wafer holder or wafers, with induction or radiant heating. The walls of the chamber remain cold (or cooler). Hot-wall systems heat the wafers, the wafer holder, and the chamber walls. The advantage of cold-wall CVD is that the reaction occurs only at the heated wafer holder. In a hot-wall system, the reaction occurs throughout the chamber, leaving reaction products on the inside chamber walls. The reaction products build up, necessitating rigorous and frequent cleaning to prevent contaminating the wafers.

CVD systems are operated with two principal energy sources: thermal and plasma. Thermal sources are tube furnaces, hot plates, and RF induction. Plasma enhanced chemical vapor deposition (PECVD) in combination with lower pressure offers the unique advantage of lowered temperatures and good film composition and coverage.

A specialty CVD used to deposit compound films, such as GaAs, is vapor phase epitaxy (VPE). A newer technique used to deposit metals is a metalorganic (MOCVD) source in a VPE system. The last deposition method described is the non-CVD molecular beam epitaxy (MBE) used for low temperature deposition of thin films in a very controlled process.

Atmospheric Pressure CVD Systems

As the name implies, atmospheric CVD system reactions and deposition take place at atmospheric pressure. There are a number of system designs that fall under this category (Fig. 12.10).

Horizontal tube—induction-heated APCVD

The first widespread use of CVD was for the deposition of silicon epitaxial films for bipolar devices. The basic system design is still used (Fig. 12.11). It is essentially a horizontal tube furnace, but with some significant differences. First the tube has a square cross section. The major difference, however, is in the heating method and wafer holder.

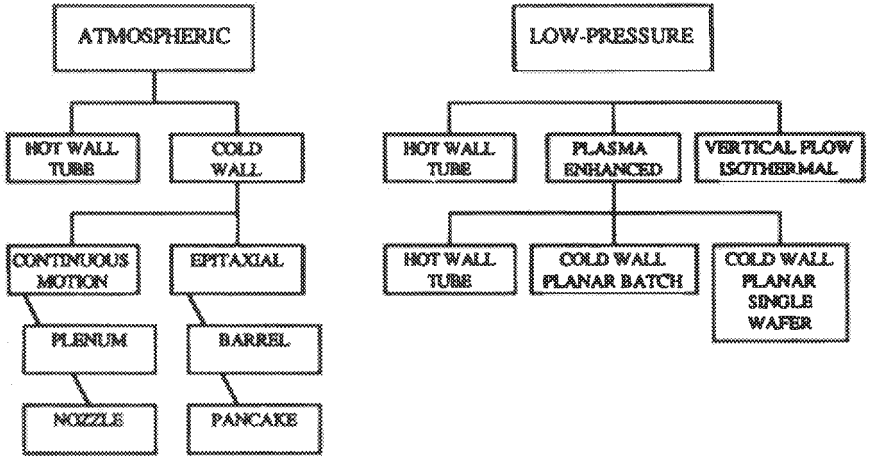


Figure 12.10 CVD reactor designs (*from Wolf and Tauber, Silicon Processing for the VLSI*)

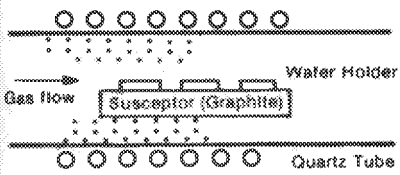


Figure 12.11 Cold-wall induction APCVD with horizontal susceptor.

Wafers are arranged on a flat graphite slab and positioned in the tube. Surrounding the tube are copper coils that are connected to an RF generator. The RF waves traveling in the coils pass through the quartz tube and the flowing gas in the tube without heating them. This is the cold-wall aspect of the system. When the radiant waves reach the graphite wafer holder, they "couple" with the molecules of the holder causing the graphite to heat up. This heating method is called *induction*.

The heat of the holder is passed to the wafers by conduction. The film deposition takes place at the wafer surface (and at the holder surface). One problem with this type of system is downstream depletion of the reactants in the laminar gas flow. Laminar flow is required to minimize turbulence. But if the wafers are laid flat in the chamber, the layer of gas closest to the wafers becomes depleted. This results in successively thinner films along the wafer holder. A wafer holder tilted in the tube corrects the problem (Fig. 12.12).

Barrel radiant-induction-heated APCVD

Larger-diameter wafers laid horizontally on a holder in a horizontal system have a low packing density. And larger wafer holders strain the uniformity capabilities of the system.

The development of the barrel radiant-heated system (Fig. 12.13) solved these problems. The reaction chamber of the system is a cylindrical stainless steel barrel with high-intensity quartz heaters placed about the inside surface. The wafers are placed on a graphite holder that rotates in the center of the barrel. The rotation of the wafers produces a more uniform film thickness compared to horizontal systems.

Radiant heat from the lamps heats the wafer surface, where the deposition takes place. While some heating of the chamber walls occurs, the system is close to a cold-wall deposition. Direct radiant heating produces a very controlled and even film growth. In an induction-heated system, the wafers are heated from the bottom, and as the film grows there is some small but measurable drop in temperature at the film surface. In the barrel system, the wafer surface is always facing

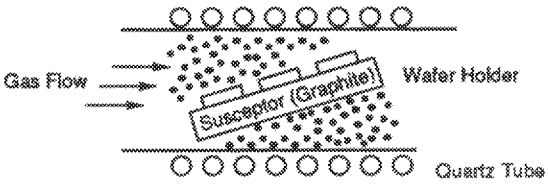


Figure 12.12 Cold-wall induction APCVD with tilted susceptor.

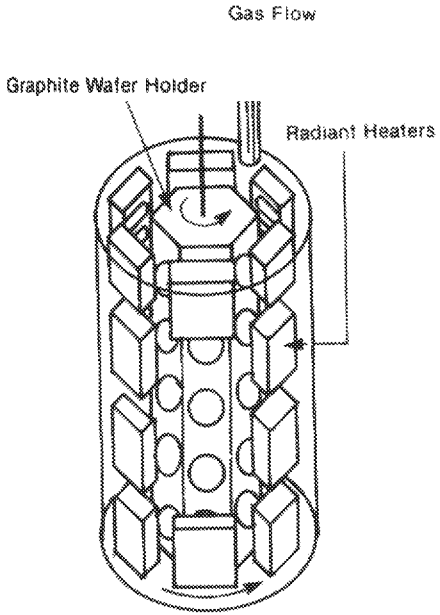


Figure 12.13 Cylindrical or barrel system.

the lamps and receives a more uniform temperature and film growth rate.

In 1987, Applied Material introduced a jumbo barrel system for large-diameter wafers featuring an induction heating system.[3] A principal advantage of the barrel reactor is an increased productivity based on the increased number of wafers per cycle. This system configuration is popular for deposition of epitaxial silicon in the 900 to 1250°C range.

Pancake induction-heated APCVD

The pancake or vertical-flow APCVD system has been a favorite for small fabrication lines and R&D labs (Fig. 12.14). The wafers are held

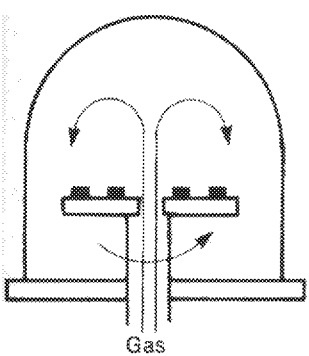


Figure 12.14 Rotating pancake APCVD.

on a rotating holder of graphite and heated by induction-conduction from an RF coil below the holder. The reaction gases are fed through a tube exiting above the wafers. Vertical gas flow offers the advantage of a continuous supply of fresh reactants to the wafers, thus minimizing downstream depletion. The combination of the rotation and vertical flow of the gases produces good film uniformity. Productivity in smaller systems is restricted, as in the horizontal tube system, by the number of wafers that the pancake can accommodate.

A production-level variation of the pancake design is produced by Gemini Research. The reactor features radiant-resistance heating and a large-capacity holder with robot autoloading.[4]

Continuous-conduction-heated APCVD

Two horizontal conduction-heated APCVD systems feature mixing the gases outside the chamber and showering them onto the wafers. In one design, a heated hot plate wafer holder moves back and forth (Fig. 12.15) under a series of nozzles that dispense a vapor of the desired material. Another version of the system (Fig. 12.16) has wafers moving on a belt under a plenum that dispenses the reacted gases.

Horizontal-conduction-heated APCVD

One of the original CVD designs is the horizontal conduction-heated APCVD system (Fig. 12.17) used to deposit the silicon dioxide passivation layers. Wafers are mounted on a removable hot plate and placed in a stainless steel chamber. The hot plate heats the wafers

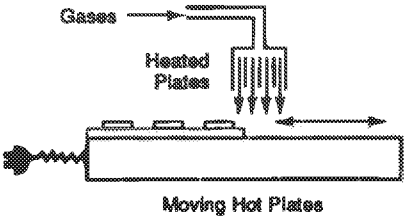


Figure 12.15 Moving hot-plate APCVD with shuttle.

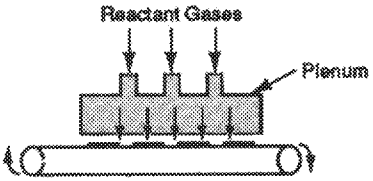


Figure 12.16 Continuous hot-plate APCVD.

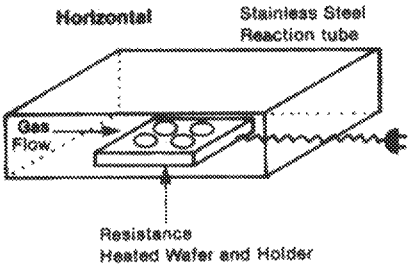


Figure 12.17 Hot-plate APCVD.

and chamber walls (hot wall system). Reaction gases are fed into the chamber.

Low-Pressure Chemical Vapor Deposition (LPCVD)

Uniformity and process control within atmospheric pressure CVD systems rely on temperature control and the flow dynamics in the system. A factor influencing film uniformity and step coverage is the mean free path of the molecules in the reaction chamber. The mean free path is the average distance a molecule will travel before colliding with an object in the chamber be it another molecule, the wafers, or wafer holder. Collisions change the direction of the particles. The longer the mean free path, the higher the uniformity of the film deposition. A major determiner of the length of the mean free path is the pressure in the system. Lowering the pressure in the chamber increases the mean free path and the film uniformity. Decreasing the pressure also allows a lowering of the deposition temperature.

These benefits became available to the industry in 1974 when Unicorp, under license to Motorola Inc., introduced an LPCVD system that operated at a few hundred millitorr.[5] The complete list of LPCVD system advantages includes:

- Lower chemical reaction temperature
- Good step coverage and uniformity
- Vertical loading of wafers for increased productivity and lower exposure to particles
- Less dependence on gas flow dynamics
- Less time for gas phase reaction particles to form
- Can be performed in standard tube furnaces

A vacuum pump must be added to the system to reduce the pressure in the chamber. A discussion of the types of pumps used with LPCVD systems is in Chapter 13.

Horizontal conduction-convection-heated LPCVD

One production-level LPCVD system uses a horizontal tube furnace (Fig. 12.18), with three major exceptions. The tube is connected to a vacuum pump that pulls the system down to a pressure range of 0.25 to 2.0 torr.[6] A second change is a ramping of the temperature in the center zone to offset reaction depletion down the tube. The third change may be special injectors at the gas inlet end to improve gas mixing and deposition uniformity. In some systems, the injectors are positioned directly over the wafers. Disadvantages of this system design are particles formed on the inside wall surface (hot-wall reactions), uniformity along the tube axis, the use of cages around the wafers to minimize particle contamination, and the higher downtime required for frequent cleaning.

These systems are most often used for polysilicon, silicon dioxide, and silicon nitride films with typical thickness uniformity's of ±5%. The primary deposition variables are temperature, pressure, gas flow, gas partial pressure, and wafer spacing. These variables are carefully balanced for each deposition process. The deposition rates are somewhat lower (100 to 500 Å/min) than AP systems, but productivity is enhanced by the vertical wafer-loading densities that can approach 200 wafers per deposition.

Ultrahigh vacuum CVD (UHV/CVD)

Low temperature deposition is desirable to minimize crystal damage and lower the thermal budget that in turn minimizes the lateral dif-

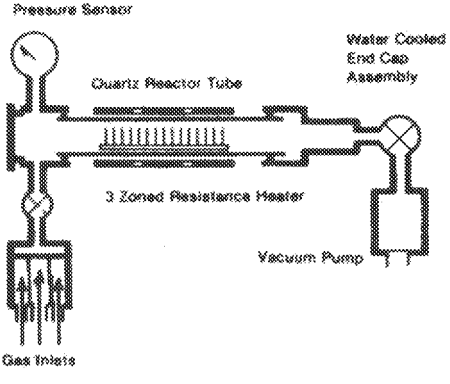


Figure 12.18 Horizontal hot-wall LPCVD system.

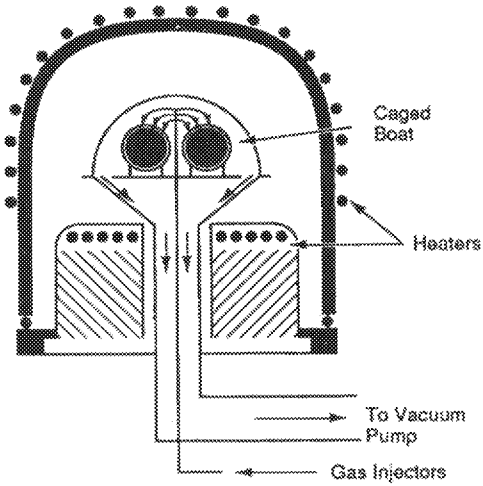


Figure 12.19 Vertical flow isotherm LPCVD. (*Courtesy of Anicon / SVG.*)

fusion of doped regions. One approach is the CVD of silicon and silicon/germanium (SiGe) in ultra low-vacuum conditions. Lowering the pressure allows keeping the deposition temperature low. UHV/CVD takes place in a tube furnace where the pressure is initially reduced to 1–5 $\times 10^{-8}$ millibar (mbar). Deposition pressure is in the 10^{-8} mbar range.[7]

Plasma-enhanced CVD (PECVD)

Replacement of silicon dioxide passivation layers with silicon nitride led to the development of PECVD techniques. A thermal silicon dioxide deposition temperature of approximately 660°C causes unacceptable alloying of aluminum interconnects into the silicon surface (see Chapter 13). A solution to this problem was a plasma enhancement of the deposition energy. The increased energy allows a temperature under the 450°C maximum level for deposition over aluminum layers. Plasma enhanced systems are physically similar to plasma etch systems. They feature a parallel plate chamber operated at a low pressure. A radio-frequency-induced glow discharge, or other plasma source (see Chapter 9) is used to induce a plasma field in the deposition gas. The combination of low pressure and lower temperatures provides good film uniformity and throughput.

PECVD reactors have the capability of also using the plasma for etching and cleaning the wafer prior to the deposition step. This step is the same as the dry etch processes described in Chapter 9. This in situ cleaning prepares the deposition surface, eliminating the problem of added contamination picked up during the loading step.

Horizontal vertical flow PECVD. This system follows the design of a bottom-heated pancake vertical-flow CVD (Fig. 12.20). The plasma region is created in the top of the chamber by a radio frequency (RF) feed to an electrode or other plasma source. Wafer heating comes from radiant heaters mounted below the wafer holder, creating a cold-wall deposition system. With PECVD systems, there are several additional critical parameters to control in addition to those in a standard LPCVD reactor. They are the RF power density, the RF frequency, and the duty cycle. Film deposition speed is generally increased, but it must be controlled to prevent film stress and/or cracking.

A single-wafer chamber PECVD system (Fig. 12.21) where the chamber is small and each successive wafer is exposed to identical conditions addresses most of the control needs. Single-wafer systems

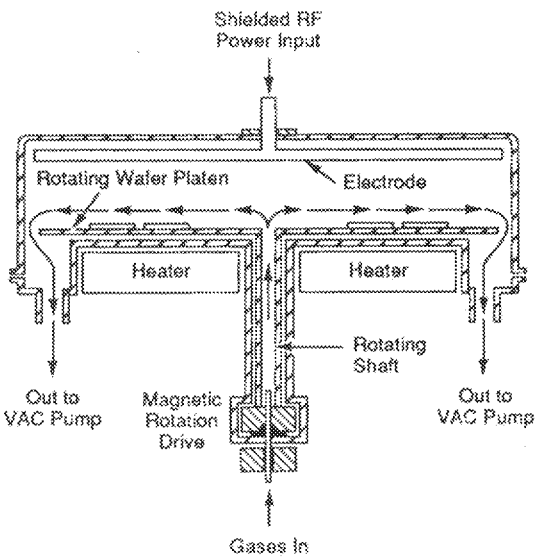


Figure 12.20 Vertical-flow pancake PECVD.

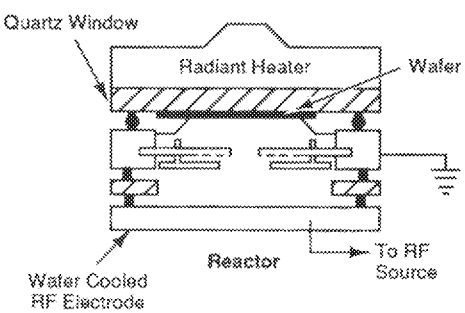


Figure 12.21 Single-chamber planar PECVD.

are generally slower than batch processes. The productivity trade-off with the larger-chamber batch machines lies in fast mechanisms to feed wafers in and out of the chamber and how quickly the vacuum can be established and released. Load-lock systems enhance the productivity by moving the wafers into an ante-chamber, pumping it down to the required pressure, and moving the wafers into the deposition chamber as it becomes available.

Barrel radiant-heated PECVD. This system is a standard barrel radiant-heated system with low pressure and plasma capabilities. It is favored for the deposition of tungsten silicide.

Horizontal-tube PECVD. This system is based on a standard tube furnace design. The plasma region is created in the specially designed wafer boat. The boat consists of slabs of graphite, alternately connected to an RF power supply (Fig. 12.22). Each pair of slabs is in effect a mini-parallel-plate plasma generator. Wafers are placed between the plates and the deposition gases passed over and through the holder where the localized plasma enhances the deposition.

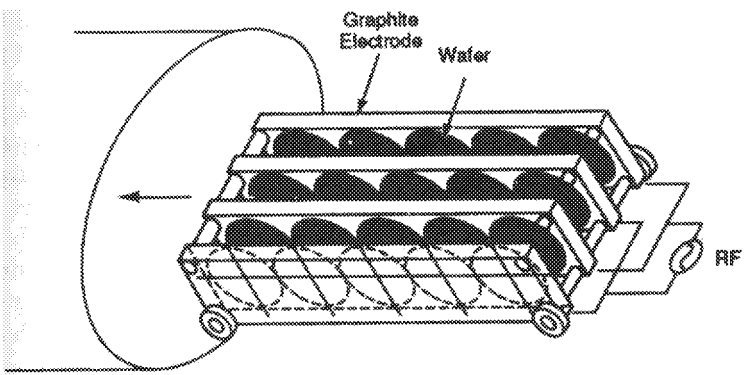


Figure 12.22 Plasma generating graphite wafer boat.

Level	Temperature Range	Methods
High Temp.	600–1250°C	R.F. Induction (Cold Wall) Radiant Heat (Cold Wall) Resistance Coils (Hot Wall)
Mid Temp..	200–600°C	Hot Plates Plasma Enhanced LPCVD
Low Range.	22–200°C	Hot Plates P.E. CVD Photochemical

Figure 12.23 Summary table of CVD methods.

Primary advantages of this approach to PECVD are the economic savings from adapting a tube furnace and high productivity. Disadvantages are in the more difficult control of the film stoichiometry and the large, heavy wafer carrier.

High density plasma CVD (HDPCVD)

Intermetal dielectric (IMD) layers are essential for multimetal structures. They also present a challenge of filling high apsect ratio (greater than 3:1) holes. One approach is a deposition and an in-situ etch sequence. The first deposition exhibits the usual thining in the bottom. Etching away the shoulder and redeposition creates an uniform layer thickness and a more planar surface.

A system to accomplish this process is high density plasma CVD.[8] A plasma field is created inside a CVD chamber that contains oxygen and silane for the deposition of silicon dioxide. Also included is argon that becomes energized by the plasma and is directed to the wafer surface. This is a sputtering ("Dry Etching," see Chapter 13) action which removes material from the surface and trench. HDPCVD has the potential of depositing a variety of materials for uses as IMD layers, etch stops, and final passivation layers.

Vapor Phase Epitaxy (VPE)

VPE differs from the CVD systems described in its ability to deposit compound materials, such as gallium arsenide. A VPE system[9] is a combination of a standard liquid source tube furnace and a two-zone diffusion furnace (Fig. 12.24). An example is the particular arrangement in Fig. 12.24 used to deposit epitaxial gallium arsenide. The creation of the GaAs layer on the wafer in the main chamber proceeds in two stages. $AsCl_3$ is bubbled into the first section of the tube where it reacts with a solid source of gallium that is sitting in a boat. The

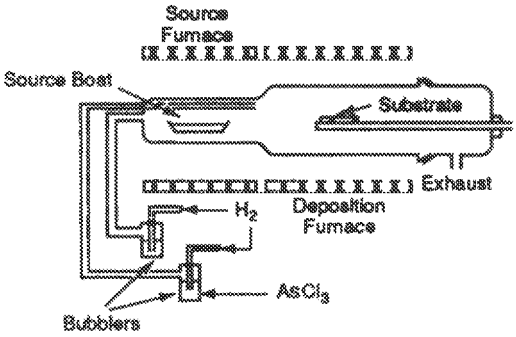


Figure 12.24 Diagram of gallium arsenide VPE deposition system.

arsenic trichloride reacts with the hydrogen in the first section to form arsenic by the reaction

$$4AsCl_3 + 6H_2 \rightarrow 12HCl + As_4$$

The arsenic deposits on the gallium forming a crust. The hydrogen passing over the crust reacts in the first section to form three gases that pass into the wafer section.

$$\underset{\text{(solid)}}{GaAs} + \underset{\text{(gas)}}{HCl} \leftrightarrow \underset{\text{(gas)}}{GaCl} + \underset{\text{(gas)}}{1/2\ H_2} + \underset{\text{(gas)}}{1/4\ As_4}$$

This section is at a somewhat lower temperature and the reaction proceeds in reverse, depositing GaAs on the wafers. The technique offers the advantages of clean films, since the gallium and arsenic trichloride are available in very pure forms and have higher production rates than the MBE technique. On the downside, the film structures produced are not the quality of MBE films.

Molecular Beam Epitaxy (MBE)

Deposition rate control, low deposition temperature, and controlled film stoichiometry are always goals in film-deposition systems. Molecular beam epitaxy (MBE) has emerged out of the laboratory to claim production status as these issues have become more important. MBE is an evaporation rather than a CVD process. The system consists of a deposition chamber (Fig. 12.25) that is maintained at a low pressure to 10^{-10} torr. Within the chamber is one or more cells (called *effusion*

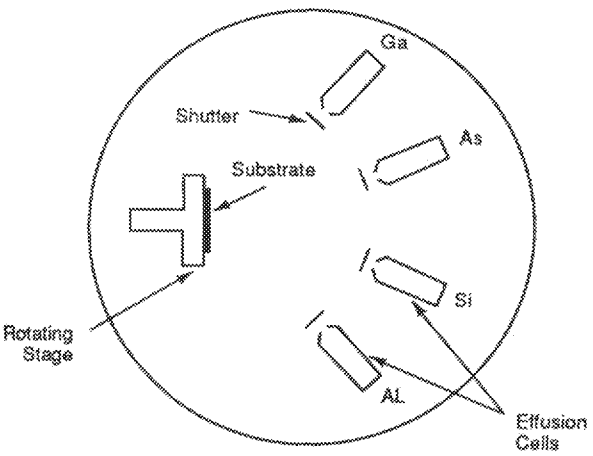


Figure 12.25 Diagram of MBE deposition system.

cells) that contain a very pure sample of the target material desired on the wafer. Shutters on the cells allow exposure of the wafer to the source material(s). An electron beam[10] is directed into the center of the target material, which it heats to the liquid state. In this state, atoms evaporate out of the material, exit the cell through an opening, and deposit on the wafers. If the material source is a gas, the technique is called *gas source MBE* or *GSMBE*. For most applications, the wafer in the chamber is heated to give additional energy to the arriving atoms. The additional energy fosters epitaxial growth and good film quality.

If the wafer surface is exposed, the depositing atoms will assume the orientation of the wafer and grow an epitaxial layer. MBE offers the intriguing option of in situ doping by the inclusion of dopant sources in the chamber. The usual silicon dopant sources are not usable in MBE systems. Solid gallium is used for P-type doping and antimony for N-type doping. Phosphorus deposition virtually not possible with MBE.[11]

The primary advantage of MBE for silicon technology is the low temperature (400 to 800°C), which minimizes autodoping and outdiffusion. Perhaps the biggest advantage of MBE is the ability to form multiple layers on the wafer surface during one process step (one pump down). This option requires the mounting of several effusion cells in the chamber and shutter arrangements to direct the evaporant beams to the wafer in the right order and for the correct time.

An advantage and disadvantage of MBE is the low film growth rate of 60 to 600 Å/min.[12] On the plus side, the films produced are very controllable. Films can be grown (and mixed) in one monolayer increments. However, most semiconductor layers do not need this level of control and quality, making the low productivity and expense of the system an expensive luxury.

A bonus possibility with MBE is the incorporation of film growth and quality-analyzing instruments in the chamber. With these instruments, the process can become very controlled and produce uniform films from wafer to wafer. MBE has found production use in the fabrication of special microwave devices and for compound semiconductors such as gallium arsenide.[13]

Metalorganic CVD (MOCVD)

MOCVD is one of the latest options for CVD of compound materials. Where VPE refers to a compound material deposition system, MOCVD refers to the sources used in VPE systems (Fig. 12.26). There are two chemistries used, halides and metalorganic. The reactions described

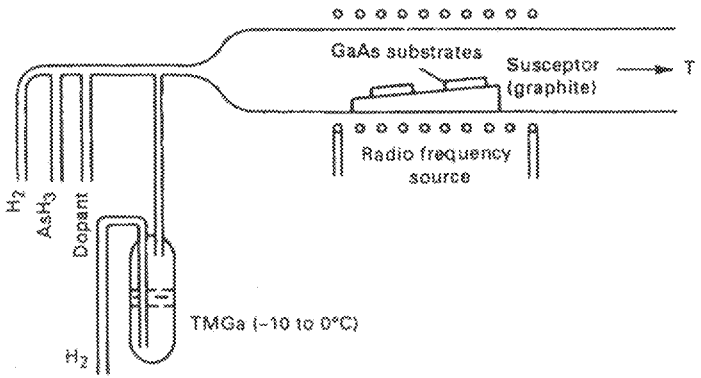


Figure 12.26 MOCVD system. (*Source: VLSI Fabrication Principles by Ghandi*)

for the VPE deposition of gallium arsenide above is a halide process. A group III halide (gallium) is formed in the hot zone and the III–IV compound is deposited in the cold zone. In the metalorganic process[14] for gallium arsenide, trimethylgallium is metered into the reaction chamber along with arsine to form gallium arsenide by the reaction

$$(CH_3)_3Ga + AsH_3 \rightarrow GaAs + 3CH_4$$

Where MBE processes are slow, MOCVD processes can meet volume production requirements and accommodate larger substrates.[15] MOCVD also has the capability of producing multiple layers with very abrupt changes in composition. This characteristic is critical to compound semiconductor structures. Also MOCVD, unlike MBE can deposit phosphorus as in InGaAsP devices. Common devices made by MOCVD processes are photocathodes, high poser LEDs, long wavelength lasers, visible laser, and orange LEDs (see Chapter 16).

MOCVD is a broad term referring to the metalorganic chemical vapor deposit of semiconductor films. When metalorganic sources are used in a vapor phase epitaxial system to grow epitaxial layers, the method is called MOVPE.[16]

Deposited Films

The types of films deposited by CVD techniques are divided into their electrical classifications of semiconductors, dielectrics, and conductors. In the following sections, the deposition of the various films is examined. For each film, its principal use(s) in semiconductor devices is presented along with the particular film properties for the described

use. The uses are treated in general. For a more detailed explanation of film roles in particular devices, see Chapter 16. Deposition methods for conductive metal films is discussed in Chapter 13.

Deposited Semiconductors

So far in this text we have discussed the formation of wafers as the base of semiconductor devices and circuits. However there are several drawbacks to using bulk wafers for high quality devices and circuits. Crystal quality, doping ranges, and doping control all limit bulk wafer use. These factors placed a limit on the fabrication of high-performance bipolar transistors. A solution was found by the development of a deposited silicon layer, called an *epitaxial layer*. It is one of the major advances in the industry. Epitaxial layers were a part of the technology as early as 1950.[17] Since then deposited silicon layers have found additional uses in advanced bipolar device design, a high-quality base for CMOS circuits, and silicon epitaxial layers deposited on sapphire and other substrates (Chapter 14). Gallium arsenide and other III–IV and II–VI films are also deposited in epitaxial films. Epitaxial films that are the same material as the substrate (silicon on silicon) are *homoepitaxial*. When the deposited material is different than the substrate (GaAs on silicon), the film is called *heteroepitaxial*.

Epitaxial Silicon

The term *epitaxial* comes from the Greek word meaning "arranged upon." In semiconductor technology, it refers to the single crystalline structure of the film. The structure comes about when silicon atoms are deposited on a bare silicon wafer in a CVD reactor (Fig. 12.27). When the chemical reactants are controlled and the system parameters set correctly, the depositing atoms arrive at the wafer surface with sufficient energy to move around on the surface and orient themselves to the crystal arrangement of the wafer atoms. Thus an epitaxial film deposited on a (111)-oriented wafer will take on a (111) orientation.

If, on the other hand, the wafer surface has a thin layer of silicon dioxide, an amorphous surface layer, or contamination the depositing atoms have no structure to align to. The resulting film structure is polysilicon. This condition is useful for some applications, such as MOS gates, and is unwanted if the goal is to grow a single-crystal film structure.

Silicon tetrachloride source chemistry. A number of different sources are used for the deposition of epitaxial silicon (Fig. 12.28). Deposition temperature, film quality, growth rate, and compatibility with a par-

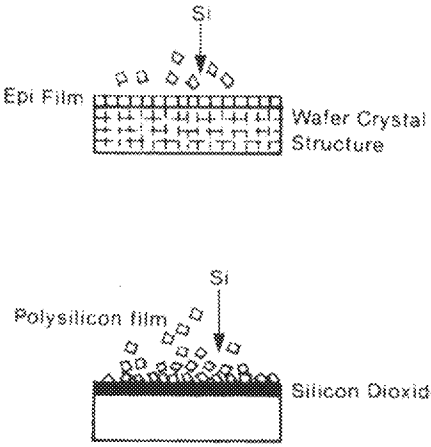


Figure 12.27 Epitaxial and polysilicon film growth.

Silicon tetrachloride	$SiCl_4 + 2H_2 \leftrightarrow Si + 4HCl$
Silane	$SiH_4 + \text{heat} \rightarrow Si + 2H_2$
Dichlorosilane	$SiH_2Cl_2 \leftrightarrow Si + 2HCl$

Figure 12.28 Epitaxial silicon chemical sources.

ticular system are factors in choosing a silicon source. An important process parameter is the deposition temperature. The higher the temperature, the faster the growth rate. Faster growth rates create more crystal defects and film cracking and stress. Higher temperatures also cause higher levels of autodoping and out-diffusion. (These effects are described in the following text.)

Silicon tetrachloride ($SiCl_4$) is the favored source of silicon for deposition is silicon. It allows a high formation temperature (growth rate) and has a reversible chemical reaction. In Fig. 12.28, there is a double-headed arrow, which indicates that the reaction creates silicon atoms in one direction and removes (etches) silicon in the other direction. Within the reactor these two reactions compete with each other.

Initially, the silicon surface is etched preparing it for the deposition reaction. In the second stage, the deposition of silicon is faster than the etch, with the net result of a deposited film.

The graph in Fig. 12.29 shows the effect of the two reactions. With an increasing percentage of $SiCl_4$ molecules in the gas stream, the deposition rate first increases. At the 0.1 ratio, the etching reaction starts to dominate and slows down the growth rate. This latter reaction is actually one of the first events in the reactor. Hydrogen chloride (HCl) gas is metered into the chamber where it etches away a thin layer of the silicon surface, preparing it for the silicon deposition.

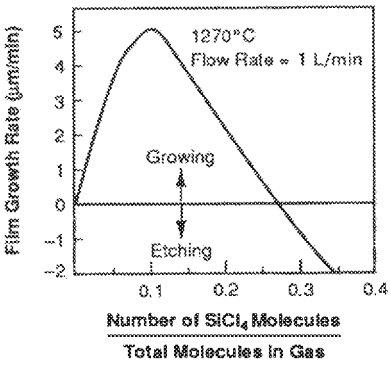


Figure 12.29 Growth-etch characteristics of $SiCl_4$ epitaxial deposition.

Silane source chemistry. The second-most-used silicon source chemistry is silane (SiH_4). Silane offers the advantage of not requiring a second reaction gas. It forms silicon atoms by decomposing when heated. The reaction takes place several hundred degrees lower than a silicon tetrachloride deposition, which is attractive from an autodoping and wafer warping perspective. Also silane does not produce pattern shift (see "Epitaxial Film Quality," p. 383). Unfortunately the reaction occurs at all locations in the system, creating a powdery film inside the reactor which, in turn, contaminates the wafers. Silane finds more use as a source for polysilicon and silicon dioxide depositions.

Dichlorosilane source chemistry. Dichlorosilane (SiH_2Cl_2) is also a lower-temperature silicon source that is used for thin epitaxial films. The lower temperature reduces autodoping and solid-state diffusion from previously diffused buried layers and provides a more uniform crystal structure.

Epitaxial film doping. One of the advantages of an epitaxial film is the precise doping and doping range available by the process. Silicon wafers are manufactured in a concentration range of approximately 10^{13} to 10^{19} atoms/cm^3. Epitaxial films can be grown from 10^{12} to 10^{20} atoms/cm^3. The upper limit is close to the solid solubility of phosphorus in silicon.

Doping in the film is achieved by the addition of a dopant gas stream to the deposition reactants. The sources of the dopant gases are exactly the same chemistries and delivery systems used in deposition doping furnaces. In effect the CVD deposition chamber is turned into a doping system. In the chamber, the dopants become incorporated into the growing film where they establish the required resistivity. Both N- and P-type films can be grown on either N- or P-type wafers.

The classic epitaxial film in bipolar technology is an N-type epitaxial film on a P-type wafer.

Epitaxial film quality. Epitaxial film quality is a prime concern of the process. In addition to the usual considerations over contamination, there are a number of faults specifically associated with epitaxial growth. Contaminated systems can cause a problem called *haze*.[18] Haze is a surface problem that varies from a microscopic disruption to severe cases that are observable as a dull matte finish. Haze comes about from residual oxygen in the reactant gases or from leaks in the system.

Contaminants on the surface at the start of the deposition result in an accelerated growth known as *spikes* (Fig. 12.30). The spikes can be as high as the film thickness. They cause holes and disruption in photoresist layers and other deposited films.

During the growth a number of crystal problems can occur. One is *stacking faults*. A stacking fault is due to the inclusion of an extra atomic plane with a corresponding "dislocation" of the atoms around the plane. A stacking fault begins at the surface and "grows" to the surface of the film. The shape of the stacking fault depends on the orientation of the film and wafer. Faults in (111)-oriented films have a pyramidal shape (Fig. 12.31), while (100)-oriented wafers form rectangular-shaped stacking faults. The faults are detected by either x-ray or etching techniques.

A growth problem associated with (111) wafers is *pattern shift*. This problem occurs when the deposition rate is too high and the film planes grow at an angle to the surface. Pattern shift is a problem when alignment to a subsurface pattern relies on locating it from a film

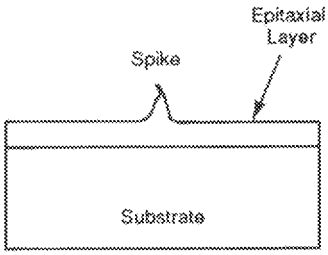


Figure 12.30 Epitaxial growth spike.

Figure 12.31 Stacking fault on (111) Si.

surface step (Fig. 12.32). Another major growth problem is *slip*. This condition comes about from poor control of the deposition parameters and results in a "slippage" of the crystal along plane interfaces (Fig. 12.33).

There are two issues associated with the temperature of the deposition: autodoping and out-diffusion. Autodoping of the growing film occurs when dopant atoms from the back of the wafer diffuse out from the wafer (Fig. 12.34), mix in the gas stream, and become incorporated into the growing film. In the film they change the resistivity and the conductivity level. *Autodoping* in a P-type film, grown over an N-type wafer, will be less P-type than intended and have a lower P-type concentration as the autodoped atoms neutralize a number of the P-type atoms in the film.

Out-diffusion causes the same effect but at the epitaxial layer-wafer interface. The source of the out-diffused atoms is doped regions diffused into the wafer before the epitaxial deposition. In bipolar devices, the regions are called *buried layers* or *subcollectors*. In the usual format, the buried layer is an N-type region in a P-type wafer, over which is grown an N-type epitaxial layer. During the deposition, the N-type atoms diffuse out and become incorporated into the bottom of the epitaxial film, changing the concentration. In the extreme, the buried layer can out-diffuse up into the bipolar device structure causing electrical malfunctions.

CMOS epitaxy. Until the late 1970s, the dominant use of epitaxial films was as the collector region of bipolar transistors. The technique provided a quality substrate for device operation and a clever means

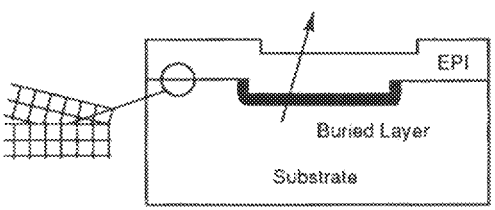


Figure 12.32 Epitaxial pattern shift.

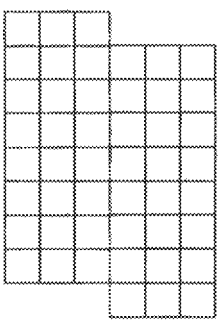
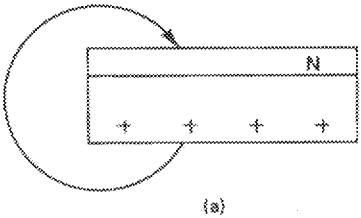


Figure 12.33 Crystal slip.



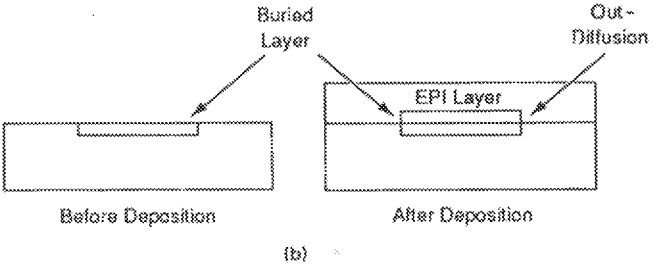


Figure 12.34 (*a*) Epitaxial autodoping and (*b*) out-diffusion.

of isolating adjacent devices (see Chapter 16). A newer and perhaps more dominant use of silicon epitaxial films is for CMOS circuit wafers. The need for an epitaxial layer was driven by a CMOS circuit problem called *latch-up* (see Chapter 16).

Epitaxial process. A typical epitaxial process starts with a complete and rigorous cleaning of the wafer surface prior to loading the reactor. Within the deposition chamber a number of steps take place to correctly deposit the film. A typical $SiCl_4$ epitaxial process is shown in Fig. 12.35. The first several steps are a gas-phase cleaning of the wafer surface. Deposition follows the cleaning with a cool-down cycle at the end. During all the steps, control of the temperature and gas flows is critical.

Cycle	Temperature	Gas	Purpose
1	Room	N_2	Purge air from system
2	Room	H_2	Reduce any organic contaminants of wafers in system
3	(Heating)	N_2	Bring system to deposition temperature
4	Deposition Temperature	HCl	Etch wafer to prepare surface for epi deposition
5	Deposition Temperature	Source + Dopant + Carrier	Grow epitaxial film
6	(Heat Off)	N_2	Purge system of reactant gases

Figure 12.35 Typical $SiCl_4$ epitaxial deposition process.

Selective epitaxial silicon. Advancement in epitaxial deposition systems has introduced the selective growth of epitaxial films. Whereas the epitaxial films for bipolar and CMOS substrates are deposited on the entire wafer, in selective growth they are grown through holes in either silicon dioxide or silicon nitride films. The wafer is positioned in the reactor chamber and the epitaxial film grows directly on the silicon exposed at the bottom of the hole (Fig. 12.36). As the film grows, it takes on the crystal orientation of the underlying wafer. An advantage of such a structure is that devices formed in the surfaces of the epitaxial regions are isolated from each other by the oxide or nitride regions.

If the deposition is allowed to continue onto the isolating surface, the structure of the film switches to a polysilicon structure. Another outcome of extended deposition is that the overlaying deposited layer becomes entirely epitaxial in nature. All of these outcomes add attractive structure options for advanced device design.

Polysilicon and Amorphous Silicon Deposition

Until the advent of silicon-gate MOS devices (Fig. 12.37) in the mid 1970s, polysilicon layers had little or no use in device structures. Silicon-gate device technology drove the need for reliable processes to deposit thin layers of polysilicon. By the mid 1980s, polysilicon seemed to be the work horse material of advanced devices. In addition to MOS

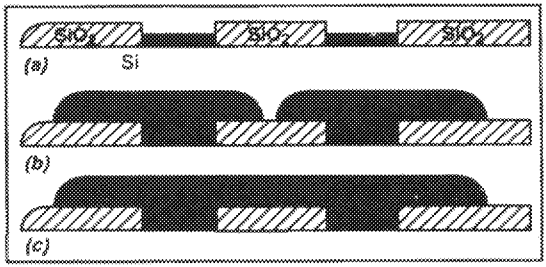


Figure 12.36 Steps in selective epitaxial growth.

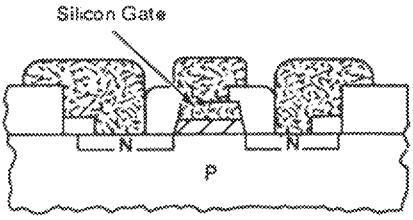


Figure 12.37 Cross section of silicon gate MOS transistor.

gates, polysilicon finds use as load resistors in SRAM devices, trench fills, multilayer poly in EEPROMs, contact barrier layers, emitters in bipolar devices, and as part of silicide metallization schemes (see Chapters 13 and 16).

Early processes involved simply placing the oxide-covered wafers in a horizontal APCVD system and letting the polysilicon deposit on the oxide. The major difference of early polysilicon depositions from epitaxial depositions was the use of silane sources. While silane is not favored for epitaxial film deposition, it is more than adequate for polysilicon depositions.

Typical polysilicon deposition processes take place in the 600 to 650°C range. The deposition may be from either 100% silane or from gas streams containing N_2 or H_2. The structure of polysilicon was previously described as a total nonarrangement of the silicon atoms. In the case of deposited polysilicon, the structure is somewhat different. During the early stages of deposition, at temperatures below 575°C, the structure is amorphous (no structure). The polysilicon structure formed by deposition techniques consists of small pockets (crystallites or grains) of single-crystalline silicon separated by grain boundaries. This structure is called *columnar poly*.

The importance of grain size and grain boundary consistency shows up in the electrical current flow characteristics of the films. Current resistance comes as the current crosses the grain boundaries. The larger the grain boundaries, the higher the resistance. The achievement of consistent current flow from device to device and within a device is dependent on a well-controlled polysilicon structure. One of the advantages claimed for the use of H_2 in the gas stream is the reduction of surface impurities and moisture, which in turn results in a reduced grain size. Moisture or oxygen impurities in the system cause the growth of silicon dioxide within the structure. The oxide increases the resistance of the film and its etchability in subsequent masking steps.

All of the system's usual operating parameters (temperature, silane concentration, pump speed, nitrogen flow, and other gas flows[19]) affect the deposition rate and the grain size. Often the wafers will receive a postdeposition anneal in the 600°C range to further crystallize the film. The process of recrystallization goes on whenever the wafers go through a high-temperature process. The grain size and electrical parameters of the polysilicon film on the finished device or circuit are never the same as the deposited film.

Also influencing the grain size is the presence of dopants in the gas stream. In many devices or circuits, a strip of polysilicon functions as a conductor which requires doping to decrease its resistivity. Doping can be done by diffusion before or implantation after the deposition.

In situ doping takes place by adding gas dopant sources in the source cabinet and metering them into the chamber. When diborane (boron source) is added, there is a large increase in the deposition rate. An opposite effect takes place when phosphine (phosphorus source) or arsine (arsenic source) is the dopant gas. Undesirable effects of in situ doping are a loss of film uniformity, doping uniformity, and control of the deposition rate.

Doped polysilicon film resistivities are less than those of equally doped epitaxial or bulk silicon. The lower resistivities are due to dopants being trapped in the grain boundaries.

Most polysilicon layers are deposited with LPCVD systems that provided good productivity and lower deposition temperatures. LPCVD provides good step coverage, a requirement since polysilicon layers are usually deposited later in the process and the surface has become varied in its topography. Single chamber polysilicon LPCVD systems offer the advantage of higher deposition rates without raising the temperature.[20]

SOS and SOI

These two acronyms stand for *silicon on sapphire* and *silicon on insulator*. Both refer to the deposition of silicon on a non semiconductor surface. The need for such structures came about from the limits placed on some MOS devices by the presence of a semiconducting substrate under the active device. These problems are resolved by forming a silicon layer on an insulating substrate. The first substrate used for this purpose was sapphire (SOS). As different substrates were inves-

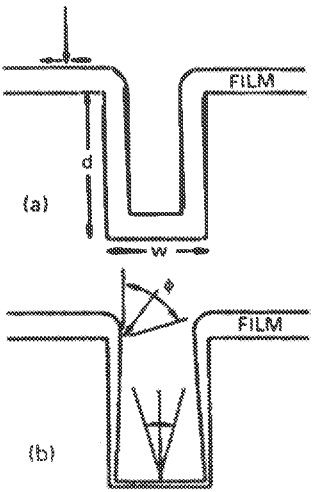


Figure 12.38 Step coverage. (*a*) good step coverage; (*b*) nonconformal coverage.

tigated, the term was expanded to the more general silicon on insulator (SOI).

One technique is a direct deposition on the substrate followed by a recrystallization process (laser heating, strip heaters, oxygen implantation) to create a usable film.[21] Another approach is a selective deposition through holes in a surface oxide with an overgrowth to form the continuous film.

Another SOI method is *SIMOX*. In this process, the top layer of a wafer is converted to oxide with a heavy oxygen implant. An epitaxial layer is grown on top of the oxide. There is some exploration of *bonded wafers*. This approach has two wafer bonded together followed by the thinning (grinding and polishing) of one to device layer thickness.[22]

Insulators and Dielectrics

CVD is the favored method of depositing films that will function in the device or circuit as insulators or dielectrics. The two films in widespread use are silicon dioxide and silicon nitride. In general, the two films find a multiplicity of uses in device and circuit designs. While they have processing and quality differences they must meet the same general requirements as other deposited films.

Silicon dioxide. Deposited silicon dioxide films are best known from their long-term use as a final passivation layer covering the completed wafer. In this role, they provide physical and chemical protection to the underlying circuit devices and components. Deposited silicon dioxide films used as a protective top layer are known by the proprietary terms *Vapox*, *Pyrox*, or *Silox*. Vapox (vapor-deposited oxide) is a term coined by Fairchild engineers. Pyrox stands for pyrolitic oxide. Silox is a registered trademark of Applied Materials, Inc. Sometimes the layer is simply called a *glass*. This protective role has expanded, and deposited silicon oxide layers are used as interdielectric layers in multimetallization schemes, as insulation between polysilicon and metallization layers, as doping barriers, as diffusion sources, as isolation regions. Silicon dioxide has become a major part of silicon gate structures. There are gate stacks, consisting of thermal oxide/silicon dioxide or oxinitride/silicon dioxide (TEOS deposited), and various silicon dioxide fillers for plugs in multimetal designs.[23]

CVD-deposited silicon dioxide films vary in structure and stoichiometry from thermally grown oxides. Depending on the deposition temperature, deposited oxides will have a lower density and different mechanical properties, such as index of refraction, resistance to cracking, dielectric strength, and etch rate. These factors are highly affected by the addition of dopants to the film. In many processes, the depos-

ited film will receive a high-temperature anneal, a process called *densification*. After the densification, the deposited silicon dioxide film is close to the structure and properties of a thermal oxide.

The need for a low-temperature-deposited SiO_2 was dictated by the unacceptable alloying of aluminum and silicon at temperatures above 450°C. The early deposition process used was a horizontal conduction-heated APCVD system from silane and oxygen by the reaction

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

This process produced films that were of unacceptable quality for use in advanced device designs and on larger wafers due to the poorer film quality produced by the 450°C deposition temperature.

The development of LPCVD systems made possible higher-quality films, especially for the factors of step coverage and lower stress. LPCVD processes are the preferred deposition techniques from both quality and productivity considerations. High temperature (900°C) LPCVD of silicon dioxide is performed with a dichlorosilane reaction with nitrous oxide.

$$SiCl_2 + 2NO_2 \rightarrow SiO_2 + 2N_2 + HCl$$

Tetraethyl orthosilicate (TEOS). By far the majority of silicon dioxide are deposited from $Si(OC_2H_5$ sources. The source is known as tetraethyl orthosilicate or TEOS. TEOS history goes back to the 1960s. Early systems relied on the simple pyrolysis of the TEOS in the 750°C range. Current depositions are based on the hot-wall LPCVD systems established in the 1970s, with temperatures the 400+°C range. TEOS sources used with plasma-assistance (PECVD or PETEOS) allowed deposition temperatures in the sub-400°C range.[24] This process faces limits on conformal coverage of high aspect ratio patterns in 0.5-μm devices. Step coverage is improved by the addition of ozone (O_3) to the gas stream.[25]

Another option is the reaction of silane with nitrous oxide in an argon plasma

$$SiH_4 + 4N_2O \rightarrow SiO_2 + 4N_2 + 2H_2O$$

Doped silicon dioxide. Silicon dioxide layers are doped to improve their protective characteristics and flow properties, or for use as dopant sources. The earliest dopant used with deposited oxides was phosphorus. The phosphorus source is phosphine (PH_3) gas added to the deposition gas stream. The resultant glass is called phosphorus silicate glass or PSG. Within the glass the phosphorus is in the form of phos-

phorus pentoxide (P_2O_5), making the glass a dual compound or, more correctly, a binary glass.

The role of the phosphorus is threefold. The added dopant increases the moisture-barrier property of the glass. Mobile ionic contaminants become attached to the phosphorus and are prevented from traveling into the wafer surface. This action is called *gettering*. The third result is an increase of the flow characteristics (Fig. 12.39) which aid the planarization of the glass surface after a heating step in the 1000°C range. The phosphorus content is limited to about 8 weight by percent. Above this level, the glass becomes hydrascopic and attracts moisture. The moisture can react with the phosphorus, form phosphoric acid, and attack underlying metal lines.

Boron is often added to the glass from a diborane (B_2H_6) source. The purpose of the boron is to also aid the flow characteristics (Fig. 12.39). The resultant glass is called a borosilicate glass (BSG). The boron and phosphorus are often used together in the glass. The result is referred to as BPSG (borophosphorus silicate glass).

Silicon nitride. Silicon nitride is a replacement for silicon dioxide uses, especially for top layer protection. Silicon nitride is harder, which provides better scratch protection, is a better moisture and sodium barrier (without doping), has a higher dielectric strength, and resists oxidation. The latter property has led to its use in the local oxidation of silicon (LOCOS) for isolation purposes. Figure 12.40 illustrates the process, where patterned islands of silicon nitride prevent oxidation under the islands. After thermal oxidation and removal of the nitride, there are wafer surface regions ready for device formation, separated by isolating regions of oxide. A disadvantage of silicon nitride is that it does not flow as easily as silicon oxide and is more difficult to etch. The etch restriction has been overcome with the development of plasma etch processes.

An early limit on the use of silicon nitride protective films was lack of a low-temperature deposition process. In APCVD systems, a tem-

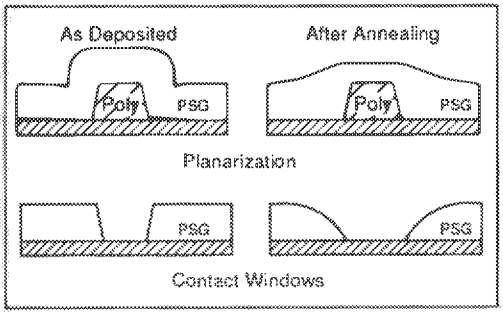


Figure 12.39 Planarization of surface by flowing glass.

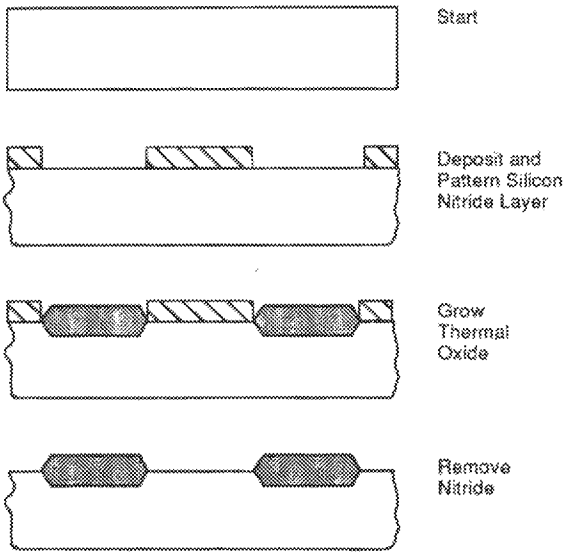


Figure 12.40 LOCOS process.

perature of 700 to 900°C is required for the deposition of silicon nitride from silane or dichlorosilane (Fig. 12.41). The result is a film with the composition Si_3N_4. The reactions also take place in LPCVD reactors but at a temperature low enough for deposition over an aluminum metallization layer. The advent of PECVD has opened up the use of different source chemistries. One use is silane reacted with ammonia (NH_3) or nitrogen in the presence of an argon plasma.

Conductors

The traditional metal conductors of aluminum and aluminum alloys deposited by evaporation or sputtering techniques. The principle deposited conductor was doped polysilicon for silicon-gate MOS transistors. The advent of multimetal structures and new conductiong materials has thrust CVD and PVD techniques into the conducting metal business. The techniques and use of these deposited metals are explained in the next chapter.

Silane	$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$
Dichlorosilane	$3SiCl_2H_2 + 4NHCl + 6H_2 + 6HCl$

Figure 12.41 Silicon nitride deposition reactions.

Key Concepts and Terms

Amorphous	MBE
APCVD	MOCVD
Barrel system	Pancake system
BPSG	PECVD
BSG	Polysilicon
CVD	PSG
Deposited Si_3N_4	Selective epitaxy
Deposited SiO_2	SOI
Epitaxial	SOS
HDPCVD	VPE
Induction heating	VPE
LPCVD	

Review Questions

1. Sketch and name the major subsystems of a basic CVD system.
2. Describe the differences between APCVD, LPCVD, and PECVD.
3. Define an epitaxial film.
4. Why is the deposition temperature of a silicon dioxide passivation layer limited to 450°C?
5. List an advantage of a horizontal vertical-flow CVD reactor.
6. Write the reaction equation for the deposition of silicon from silicon tetrachloride.
7. Describe the difference between MBE, VPE, and MOCVD systems.
8. What wafer surface condition is necessary for the deposition of a polysilicon layer?
9. Describe the advantages of plasma-assisted depositions compared to APCVD systems.
10. Why, and with what, are deposited silicon dioxide layers doped?

References

12.1 J. Hayes and P. Van Zant, *CVD Today Seminar Manual, Semiconductor Services*, San Jose, CA, 1985, p. 9.
12.2 S. Wolf and R. Tauber, *Silicon Processing for the VLSI Era*, Lattice Press, Sunset Beach, CA, 1986, p. 165.

12.3 M. L. Hammond, "Epitaxial Silicon Reactor Technology: A Review," *Solid State Technology*, May 1988, p. 160.
12.4 M. L. Hammond, "Epitaxial Silicon Reactor Technology: A Review," *Solid State Technology*, May 1988, p. 160.
12.5 J. Hayes and P. Van Zant, *CVD Today Seminar Manual*, Semiconductor Services, San Jose, CA, 1985, p. 13.
12.6 S. Wolf and R. Tauber, *Silicon Processing for the VLSI Era*, Lattice Press, Sunset Beach, CA, 1986, p. 165.
12.7 B. Meyerson, H. Kaiser, and S. Schultz, "Extending Silicon's Horizon through UHV/CVD," *Semiconductor International*, Cahners Publishing, March 1994, p. 73.
12.8 P. Singer, "The Future of Dielectric CVD: High Density Plasma?," *Semiconductor International*, July 1997, p. 127.
12.9 R. Williams, *Gallium Arsenide Processing Techniques*, Artech House, Dedham, Mass., 1984, p. 44.
12.10 S. Wolf and R. Tauber, *Silicon Processing for the VLSI Era*, Lattice Press, Sunset Beach, CA, 1986, p. 157.
12.11 P. Burggraaf, "The Status of MOCVD Technology," *Semiconductor International*, Cahners Publishing, July 1993, p. 81.
12.12 P. Singer, "Molecular beam epitaxy," *Semiconductor International*, Oct 1986, p 42.
12.13 P. Burggraaf, "The Growing Importance of MOCVD," *Semiconductor International*, November 1986, p. 47.
12.14 P. Burggraaf, "The Growing Importance of MOCVD," *Semiconductor International*, November 1986, p. 48.
12.15 P. Burggraaf, "The Status of MOCVD Technology," *Semiconductor International*, Cahners Publishing, July 1993, p. 81.
12.16 A. Thompson, R. Stall, and B. Droll, "Advamces om Epitaxial Deposition Technology," *Semiconductor International*, Cahners Publishing, July 1994, p. 173.
12.17 M. L. Hammond, "Epitaxial Silicon Reactor Technology: A Review," *Solid State Technology*, May 1988, p. 159.
12.18 R. P. Roberge, et al., "Gaseous Impurity Effects in Silicon Epitaxy," *Semiconductor International*, January 1988, p. 81.
12.19 S. M. Sze, *VLSI Technology*, McGraw-Hill, New York, 1983, p. 119.
12.20 M. Venkatesan and I. Beinglass, "Single-wafer Deposition of Polycrystalline Silicon," *Solid State Technology*, Penwell Publishing, March 1993, p. 49.
12.21 L. Jastrzebski, "Silicon CVD for SOI: Principles and Possible Applications," *Solid State Technology*, September 1984, p. 239.
12.22 K. Yallup, "SOI Provides Total Dielectric Isolation," *Semiconductor International*, Cahners Publishing, July 1993, p. 134.
12.23 P. Singer, "Directions in Dielectrics in CMOS and DRAMs," *Semiconductor International*, Cahners Publishing, April 1994, p. 57.
12.24 B. L. Chin and E. P. van de Ven, "Plasma TEOS Process for Interlayer Dielectric Applications," *Solid State Technology*, April 1988, p. 119.
12.25 K. Maeda and S. Fisher, "CVD TEOS/O3: Development History and Applications," *Solid State Technology*, Penwell Publishing, June 1993, p. 83